

ABSTRACT OF THE DISCLOSURE

An active area (1) is provided with a concave part in its corner portion in a shape along a plan view. An insulating film (7) encloses this active area. A gate electrode (30) is arranged on a depressed region (DR) having an edge portion which is located on a low position due to the concave part, while a gate electrode (20) is arranged on an ordinary region (OR) having an edge portion projecting beyond the depressed region. A gate end cap (margin part) of the gate electrode (20) has a length x , while that of the gate electrode (30) has a length $x + \alpha$. Thus provided is a semiconductor device causing no current defect between source/drain regions even if the active area and an insulating film defining this active area fail to satisfy the layout design following refinement of the semiconductor device.

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